



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yeo, *et al.*

Docket No.: TSM03-0421

Serial No.: 10/608,287

Art Unit: 2891

Filed: June 27, 2003

Examiner: Chaudhari, Chandra P.

For: Structure and Method for Forming the Gate Electrode in a Multiple-Gate Transistor

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A & B that may be considered material to the examination of the above-identified application. Copies of the U.S. Patents cited are not being submitted. However, Applicant has included copies of the foreign patents and non-patent literature.

This Information Disclosure Statement is submitted under 37 C.F.R. §1.97(c) together with a \$180.00 fee under 37 C.F.R. §1.17(p) after the C.F.R. §1.97(b) time period, but before final action or notice of allowance, whichever occurs first. Please charge the required fee of \$180.00 and any additional amount, or credit any overpayment to Deposit Acct. No 50-1065 of the below mentioned firm. A duplicate copy of this sheet is enclosed.

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June 22, 2005

Date

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Respectfully submitted,

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(Use as many sheets as necessary)

Application Number	10/608,287
Filing Date	June 27, 2003
First Named Inventor	Yeo, <i>et al.</i>
Art Unit	2891
Examiner Name	Chaudhari, Chandra P.
Attorney Docket Number	TSM03-0421

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>			Complete if Known		
			Application Number	10/608,287	
			Filing Date	June 27, 2003	
			First Named Inventor	Yeo, et al.	
			Art Unit	2891	
			Examiner Name	Chaudhari, Chandra P.	
Sheet	2	of	4	Attorney Docket Number	TSM03-0421

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
	23	US-6,475,890 B1	11-05-2002	Yu	
	24	US-6,476,437 B2	11-05-2002	Liaw	
	25	US-2003/0011080 A1	01-16-2003	Deshpande et al.	
	26	US-6,514,808 B1	02-04-2003	Samavedam et al.	
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	47	US-2004/0119100 A1	06-24-2004	Nowak et al.	
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				Application Number	10/608,287
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				Examiner Name	Chaudhari, Chandra P.
				Attorney Docket Number	TSM03-0421
Sheet	3	of	4		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	48	AUTH, C.P., et al., "Scaling Theory for Cylindrical, Fully-Depleted, Surrounding-Gate MOSFET's," IEEE Electron Device Letters, Vol. 18, No. 2 (February 1997) pp. 74-76.	
	49	CELIK, M., et al., "A 45 nm Gate Length High Performance SOI Transistor for 100nm CMOS Technology Applications," Symposium on VLSI Technology Digest of Technical Papers (2002) pp. 166-167.	
	50	CHAU, R., et al., "A 50nm Depleted-Substrate CMOS Transistor (DST)," IEDM (2001) pp. 621-624.	
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	55	JE, M., et al., "Quantized Conductance of a Gate-All-Around Silicon Quantum Wire Transistor," Microprocesses and Nanotechnology Conference (1998) pp. 150-151.	
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	58	OH, S-H., et al., "Analytic Description of Short-Channel Effects in Fully-Depleted Double-Gate and Cylindrical, Surrounding-Gate MOSFETs," IEEE Electron Device Letters, Vol. 21, No. 9 (September 2000) pp. 445-447.	

Examiner Signature		Date Considered	
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